CMPT 880/479
Multicore Programming and Architecture

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Unit 1: Performance Tuning

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Today's Agenda

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- Why all this talk about sequential performance?
  - Seldom taught
  - Even more rarely practiced in coursework
  - Key foundation for efficient parallel code

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- Lecture on sequential performance tuning
  - Overview, much of it should be review
  - Help you tune code
  - Help you understand odd performance effects

The Process of Performance Tuning

Goals of Performance Tuning

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- Or, **energy consumption**
  - Same computation, less energy
  - Why? **battery life, power & cooling costs, fan noise**
  - Run fast and sleep **--or--** run slowly just to meet deadlines

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  - Same computation, less energy
  - Why? **battery life, power & cooling costs, fan noise**
  - Run fast and sleep **--or--** run slowly just to meet deadlines
- Either way: **software tuning basically the same**
  - In fact, processors dynamically trade energy and performance
    - Dynamic voltage/frequency scaling, Core i7 "turbo mode"

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  - 2. benchmark and profile, identify bottleneck
  - 3. Modify code, test functionality, measure perf., revert if not beneficial
  - Ongoing performance regression testing

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- **Performance optimization**: empirical & experimental
  - 1. wait
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  - 3. Modify code, test functionality, measure perf., revert if not beneficial
  - Ongoing performance regression testing
- "We should forget about small efficiencies, say about 97% of the time: **premature optimization is the root of all evil**"
  - Donald Knuth

Identifying Performance Bottlenecks

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- **Where is the code spending its time?**
  - Need representative input (full sized, long running)
  - Various profiling tools (gprof, Valgrind's cachegrind, Intel's VTune)
  - Look beyond code profile (collect by object, algorithm change, etc.)

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- **Hardware performance counters**
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  - Can even associate them with specific instructions
  - Using sampling, can be done with low overhead (a few percent)

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  - Using sampling, can be done with low overhead (a few percent)
- **Focused experiments** (example: large v. small data set)

Performance Tuning of Sequential Code

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- Fast parallel code is fast sequential code running in parallel
- Runtime = # of inst. * cycles per inst. * clock period
  - Want to minimize all three
- When tuning code, consider:
  - "Dynamic" instruction count
  - Micro-architectural impacts
    - Instruction level parallelism of code, branch mispredictions
  - Memory hierarchy
    - Cache misses, etc.

Reducing Instruction Count

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- **Reducing instruction count**
  - Better algorithm or approach to problem
  - Avoid software bloat in terms of too much layering, too general
  - Write code the compiler can easily optimize (and turn on -O3)
    - Compilers are really smart, but lack higher level context

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  - After a call, compiler doesn't know what has changed or not
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- Aside: "extern inline" function in .h file is a fast as a macro

Operation & Instruction Latencies

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- Instruction latencies
  - One cycle: integer adds, subtract, compare, shift, etc.
  - Few cycles: loads/stores (best case), int multiply, floating point
  - Dozens of cycles: integer divide (89 cycles for 64-bit on Core i7)

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- Non-instructions (on most machines)
  - Sqrt, exponentiation, sine/cosine, modulo (%), etc.
  - Trend toward more hardware support for these operations
- Compilers can by help
  - Selects cheapest instructions (strength reduction)
    - Replace multiply by constant power-of-two with shift: "x * 2" with "x << 1"
  - Tries to eliminate redundant computation

Tuning for Micro-Architectural Impacts

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- Superscalar execution: three or four insn per cycle max
  - Restrictions on instruction mix (different function unit types)
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- Loop accelerators (if loop body is <N insn, goes faster)

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int distance(int a, int b)
{
  return (a > b) ? a-b : b-a;
}
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gcc -m32 -O3

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distance:
   pushl %ebp
   movl  %esp, %ebp
   movl  8(%ebp), %edx
   movl  12(%ebp), %eax
   cmpl  %eax, %edx
   jg    .L6
   subl  %edx, %eax
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.L6:
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gcc -m32 -march=core2 -O3

```
distance:
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   movl   %edx, %ebx
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gcc -m64 -O3

```
distance:
   movl   %edi, %eax
   movl   %esi, %edx
   subl   %esi, %eax
   subl   %edi, %edx
   cmpl   %esi, %edi
   cmovle %edx, %eax
   ret
```

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```

- Note: only works (on x86) for non-memory operations
  - Why? Must ensure the memory operation won't seg fault

Code Example II

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        movl    (%rdx,%rax,4), %esi
  .L2:
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- Comments on x86 assembly
  - Right-most register is usually the output register
  - "mov" instructions are loads, stores, or register copies
    - Memory access is indicated by "(...)"
  - "%exx" are 32-bit registers, "%rxx" are 64-bit registers
  - movslq: "sign extending" a "long" (32-bit) to a quad (64-bit)

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int func2(int a, int b, int* array)
{
  int temp = array[b];
  return (a > 0) ? b : temp;
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What Can the Compiler Do or Not Do?

```
void loop(int64 n, int64* array1, int64* array2, int64* ptr)
{
  for (int i = 0; i < n; i++) {
    for (int j = 0; j < n; j++) {
      if (*ptr > array2[j]) {
        array1[i] += array2[j];
      }
    }
  }
}
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- How might you rewrite the code to help?

Code Example III

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void loop(int64 n, int64* array1,
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  for (int64 i = 0; i < n; i++) {
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}
```

Inner loop of loop()

```
.L5:  movq  (%rdx,%rax,8), %r8
      cmpq  %r8, (%rcx)
      jle   .L4
      addq  %r8, (%rsi,%r9,8)
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load, add, store

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{
  for (int64 i = 0; i < n; i++) {
    int64 accumulator = 0;
    for (int64 j = 0; j < n; j++) {
      if (*ptr > array2[j]) {
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    }
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Inner loop of loop2()

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      cmpq  %r10, %r8
      jge   .L12
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Inner loop of loop2() + CMOV

```
.L14: movq  (%r11,%r8,8), %rax
      leaq  (%r9,%rax), %rdx
      cmpq  %r10, %rax
      cmovl %rdx, %r9
      addq  $1, %r8
      cmpq  %r8, %rdi
      jg    .L14
```

not a load!

Aside: Profile-Based Compilation

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  - <run program>
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  - gcc -fprofile-generate ...
  - <run program>
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- Helps compiler:
  - Know which way branches commonly go
  - Frequency of loops (loop unrolling, loop peeling, etc.)

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  - <run program>
  - gcc -fprofile-use ...
- Helps compiler:
  - Know which way branches commonly go
  - Frequency of loops (loop unrolling, loop peeling, etc.)
- Good just-in-time (JIT) compilers do this automatically

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- Example: is a binary tree or an N-array tree more efficient?
  - Binary tree nodes are small (low spatial locality)
  - Binary trees do lots of pointer indirections

More Information

- "Intel 64 and IA-32 Architectures Optimization Reference Manual"
  - http://www.intel.com/Assets/PDF/manual/248966.pdf
- "Software Optimization Guide for AMD Family 10h Processors"
  - http://www.amd.com/us-en/assets/content_type/white_papers_and_tech_docs/40546.pdf
- "man gcc" for compiler flags
- "What Every Programmer Should Know About Memory"
  - Ulrich Drepper, http://people.redhat.com/drepper/cpumemory.pdf
- "Instruction latencies and throughput for x86 processors"
  - Torbjorn Granlund, http://gmplib.org/~tege/x86-timing.pdf
- "x86-64 Machine-Level Programming"
  - Bryant & O'Hallaron,
  - http://www.cs.cmu.edu/~fp/courses/15213-s06/misc/asm64-handout.pdf

Low-Level Tuning of Parallel Code

Multicore Organization

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  - Memory controllers for directly connect memory chips (DRAM)
- Multiple sockets per system
  - Dual-socket servers standard for years
  - Quad-socket becoming common (from AMD & Intel)
  - Large systems with hundreds of sockets have been built
  - Today, usually no caching shared among sockets

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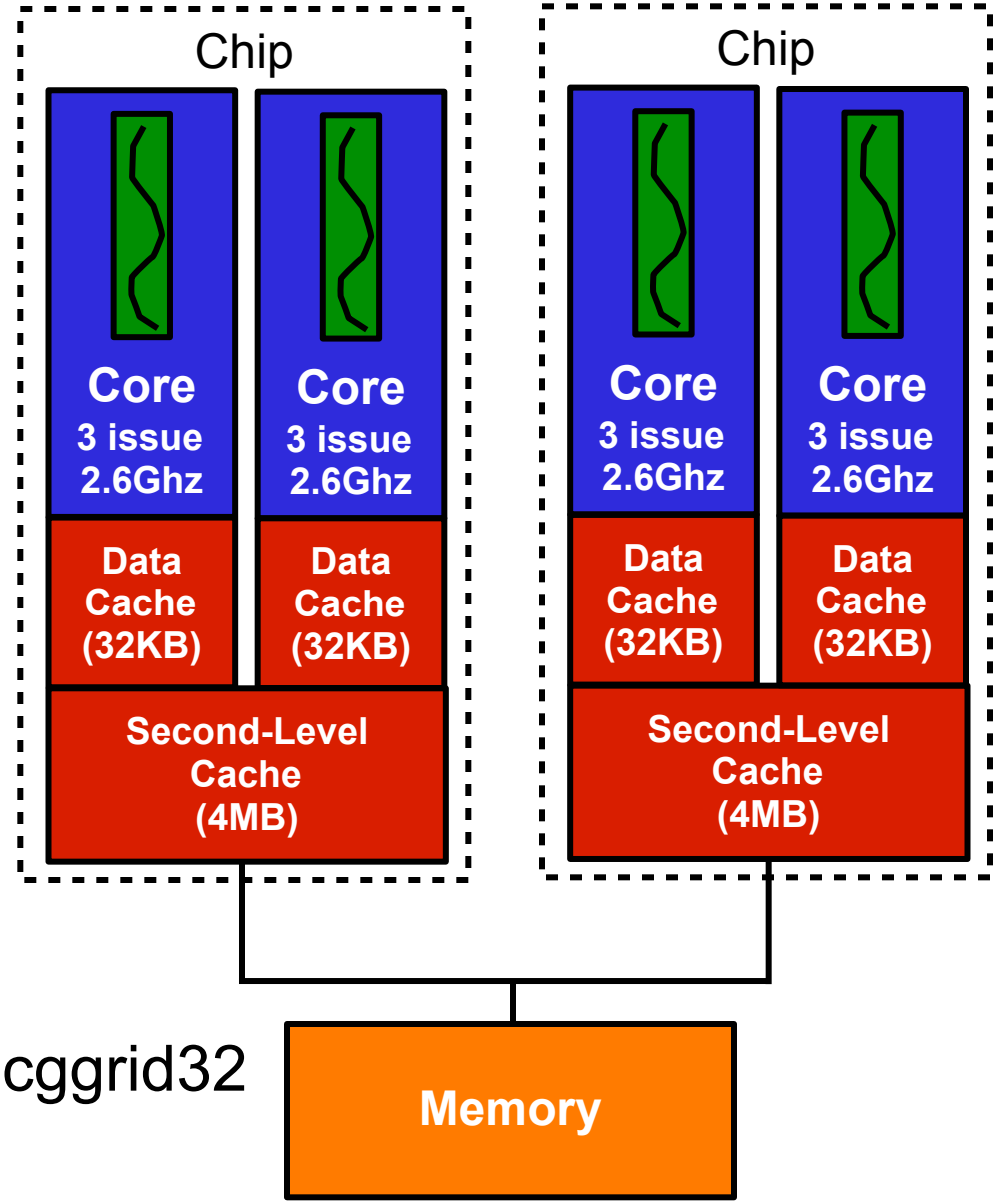
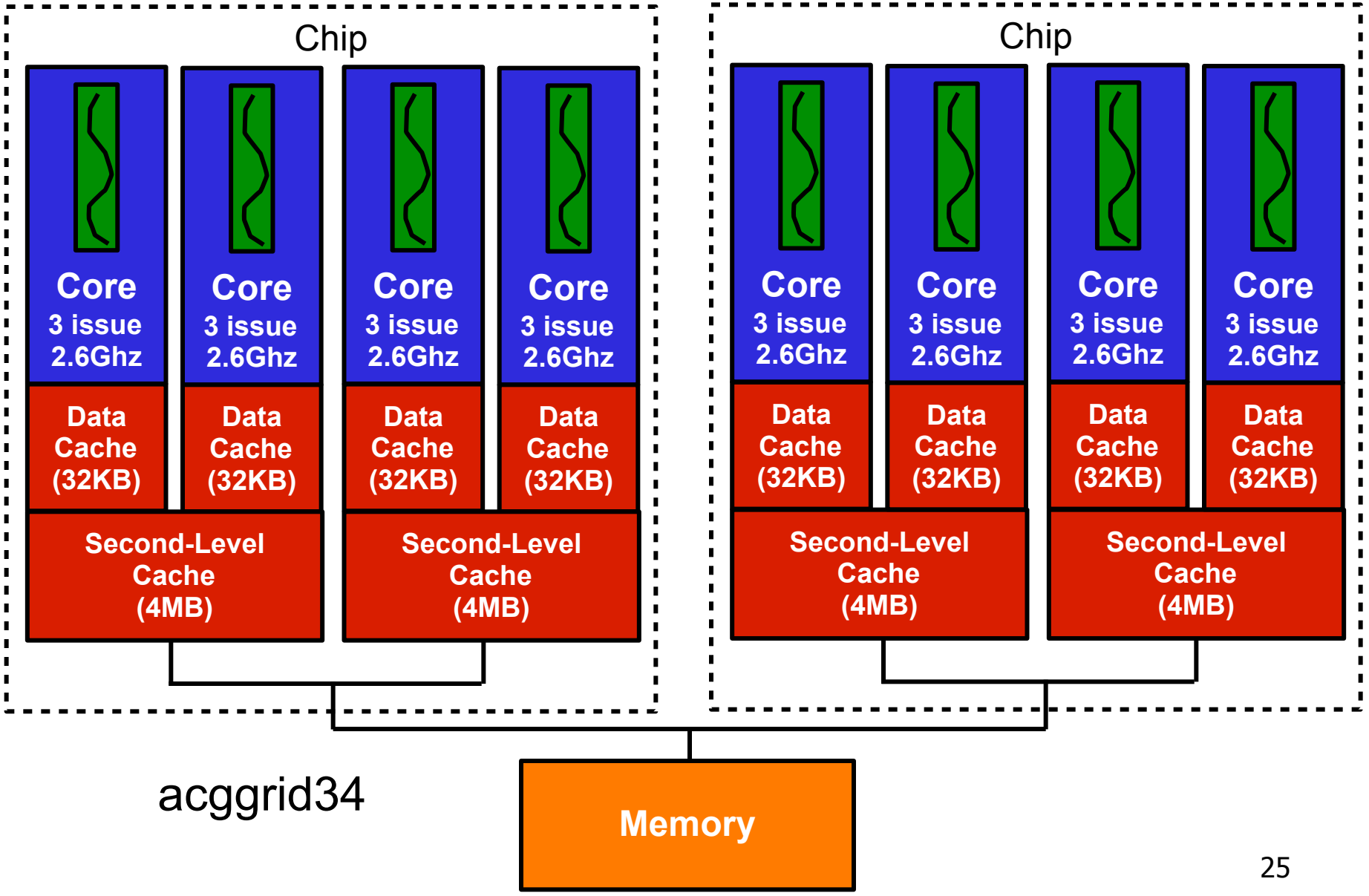
- Page mapping controlled by OS
  - To optimize for lowest latency:
    - All local pages
  - To optimize for highest bandwidth:
    - Distribute pages to use all memory controllers
  - What happens in practice? oblivious allocation probably does okay

Dual-Socket Dual-Core "Core 2"



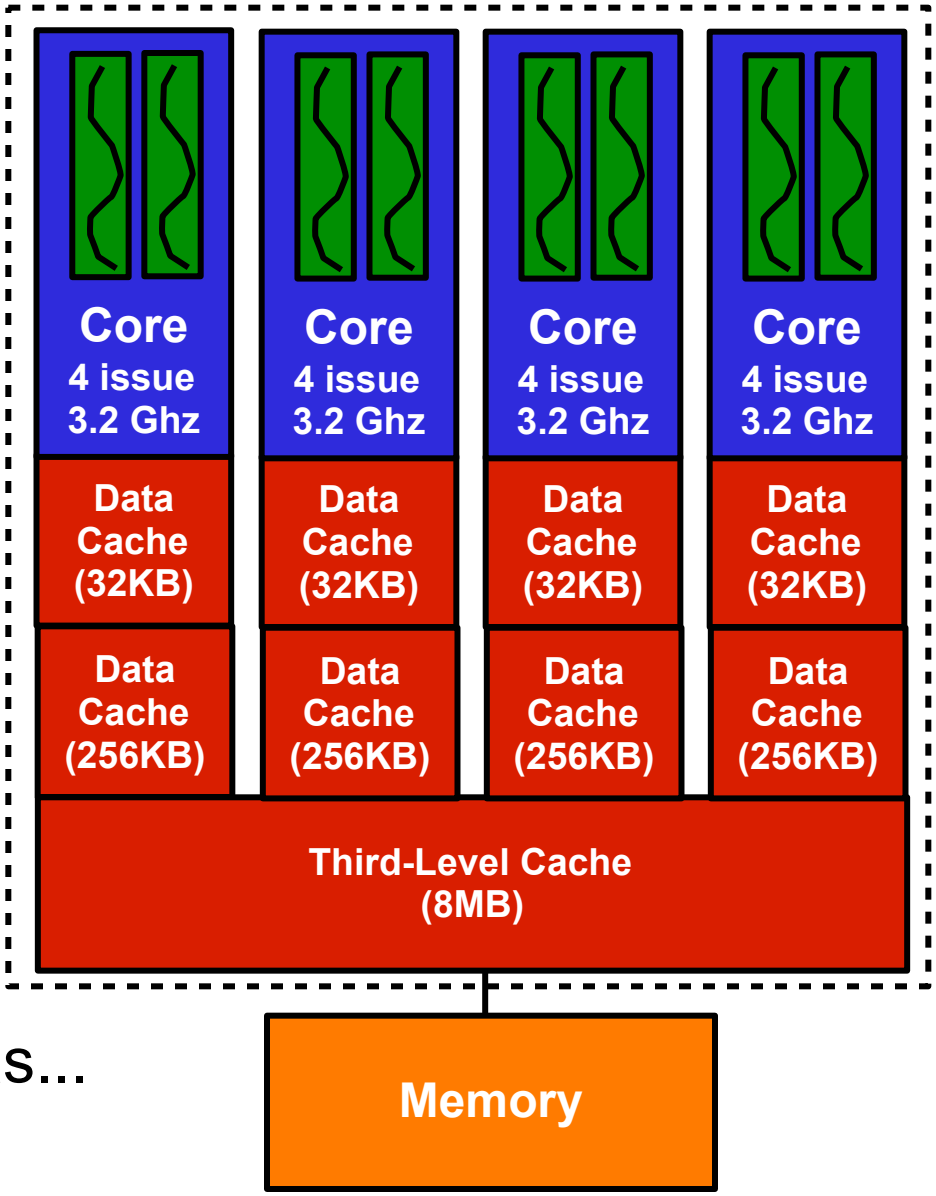
acggrid01 - acggrid32

Dual-Socket Quad-Core "Core 2"



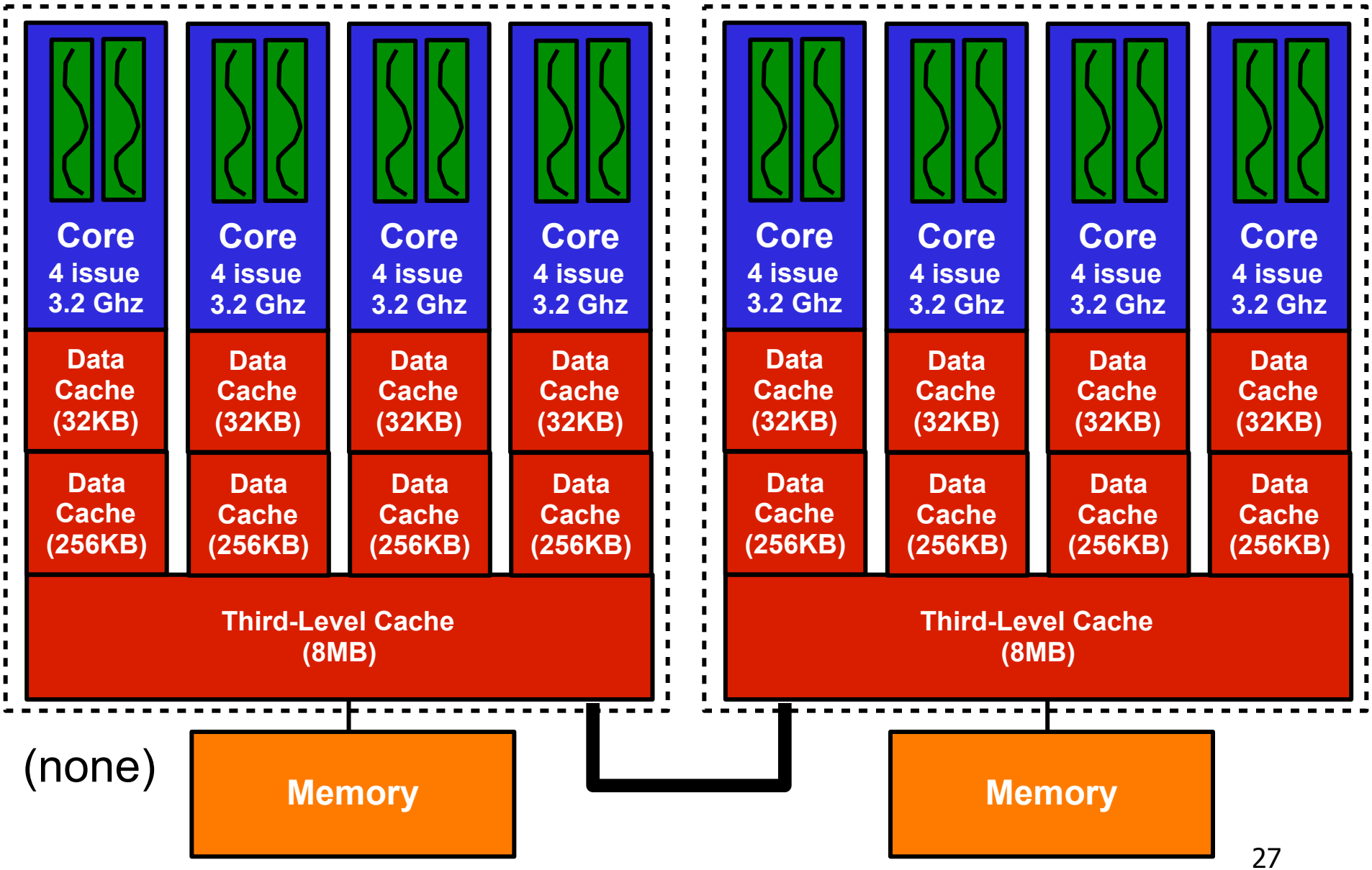
acggrid34

Single-Socket Quad-Core "Core i7"

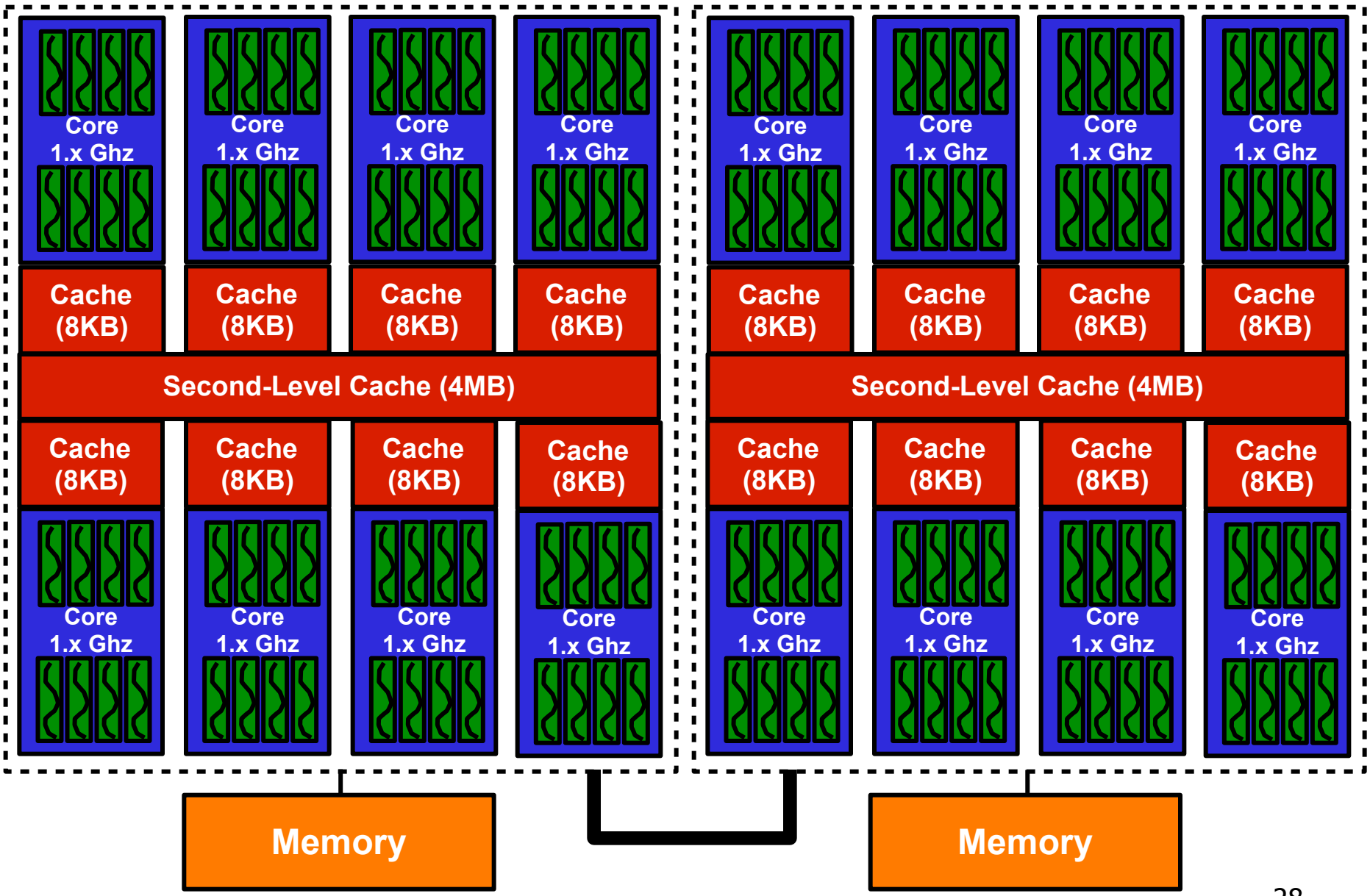


acggrid35.seas...

Dual-Socket Quad-Core "Core i7"



Dual-Socket Oct-Core "Niagara T2"



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- Performance implication: sharing is slow
  - Slower off-chip sharing than on-chip sharing

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  - **Take away: avoid read/write sharing of data**
- False sharing
  - If two variables fall in the same cache block, block may ping-pong
  - Example: Each core increments "own" counter in an array
    - Repeatedly fetch and invalidate block -> **extremely slow**
  - Possible solutions:
    - Manually pad data to ensure they are in different cache blocks
    - malloc() could align each object to 64B boundaries

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  - Multithreading hides lots of miss latency!
- Negative
  - **Higher miss rates**
    - More threads all trying to use limited shared cache capacity
      - Impact depends on data locality among threads
    - Sharing misses
  - **High miss latencies**
    - Sharing misses are often slower
    - Perhaps missing to other socket's memory
  - **More memory bandwidth bottlenecks**
    - Many parallel misses trying to use limited memory bandwidth
    - Adding memory bandwidth is expensive, so big concern

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- Review of synchronization, locks and barriers
  - Shared memory/multithreaded coding
  - Synchronization primitives