Lecture 34
July 30
Exam

- Similar format to midterm
  - Some multiple choice
  - Long answer
- 3 hours
  - 2X length of mid term
- cumulative
  - slight emphasis on 2nd half
  - include VHDL & reading
  - cache
  - bonus question 1 mark out of 90

Multiple Cycle Control
The life of an instruction

- PC points to next instruction
- Instruction fetch (IF)
  - Microinstruction in address 192 of control ROM
  - So the CAR should have 192
  - Must load IR with instruction from memory
    - IL = 1
    - MM = 1
    - MW = 0
    - RW = 0
  - Must then start the execution of micro program (EXO)
    - Need to increment CAR
      MS = 000must increment PC
      - PI = 1
      - Pl = 0
  - EXO: start the execution
    - Need to start the micro-program for the opcode
      - Its micro program will always start at 0||opcode
      - Load CAR with 0||opcde
        - MS = 001
        - MC =1
    - Nothing else should change
      - MW = 0
      - RW = 0
      - IL = 0
      - PI = 0
      - PL = 0

- Instruction execution
  - Run the actual micro program to implement the given opcode
  - E.g. ADD (register read)
    - Do the addition:
      - TA = 0
      - TB =0
      - MB = 0
      - FS = 00010
    - Write back to DR:
      - MD = 0
      - TD = 0
      - RW =1
    - Don’t change memory:
      - MW = 0

– Next, go back to IF micro instruction(this is the last instruction of all micro program)
  - Load CAR with 192
    - MS = 001
    - NA = 192
    - MC = 0
  - Don’t update the registers:
    - PI = 0
    - PL = 0
    - IL = 0