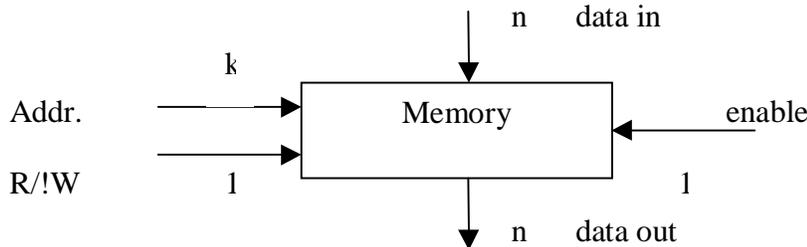Lecture 25
July 9

RISC continue
- With all this taken into account, a RISC processor will be several times faster
    - o Assuming other facors are the same
    - o Modern CISC prcessors borrow many RISC ideas to gain speed

Memory
- Most processors can have a memory attached

- o When R/!W is 0, the data will load into the location indicated by addr.
- o When R/!W is 1, send the value in memory location out dat out
- Works a lot like a register file
    - o It could be implemented as a collection of registers
        - ▪ "static RAM" (SRAM)
        - ▪ expenseive
    - o bits could also be represented with capacitors
        - ▪ charged capactor → 1 discharged →
        - ▪ "dynamic RAM" (DRAM)
        - ▪ cheaper but slower
- DRAM must be periodically "refreshed"
    - o As the charge in the capacitor discipates, it must be recharged
    - o Other wise 1's turn into 0's
- PC's use DRAM
    - o SDRAM: synchronous DRAM
        - ▪ Activated by a clock signal.
    - o DDR RAM: double-data rate RAM
        - ▪ SDRAM that is activated by the rising and falling clock edges
    - o RAM is typically 5-10X slower than the processor
        - ▪ Ie. It takes 5-10 clock cycle to do a R/W
- If we have to wait 6 clock cycles for each memory access, it's going to slow the processor down
    - o A load-store architecture will have an advantage
    - o Must still do instruction fetches

Memory Hierarchy
- There are three main ways to store information in
    - Computer: registers, memory, hard disk
        - There one large speed differences between them:
            - Registers → memory: 5-10X
            - Memory → hard disk 10^5 X
        - Also larget difference in capacity
            - Registers ~ 10 words
            - Memory ~ 10^8 words
            - Hard disk ~ 10^11 words
- We often have the problem of insufficient storage space in registers or RAM
    - We move info to the next fastest storage
        - Registers → memory
        - Memory → disk
    - Registers s<-->RAM is handled by the programmer
    - Memory <--> hard disk is handled by the OS
    - Done transparently – user/programmer never see it happen
    - "virtual memory"
- We can also help with the relative speed problem
    - the solution: caching