Sequence control

NA: next control Address

- IC CAR loads, its used
- Which micro-instruction next?
- In the last cycle, this is the control address of IF

MS:

- Decide if CAR increments or loads
    - if MUXS outputs 0 increment; 1 load
    - MS=001 → always load

MC: CAR loads from NA (0) or 0|| opcode (1)

- Set to 1 only by EXO
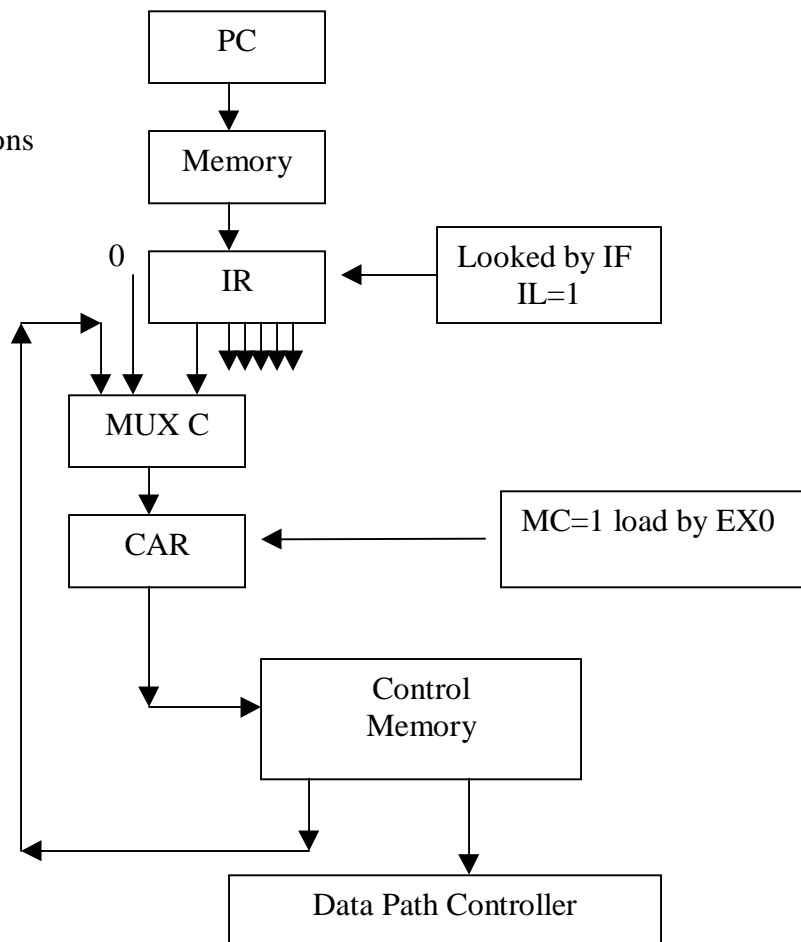
IL: load IR

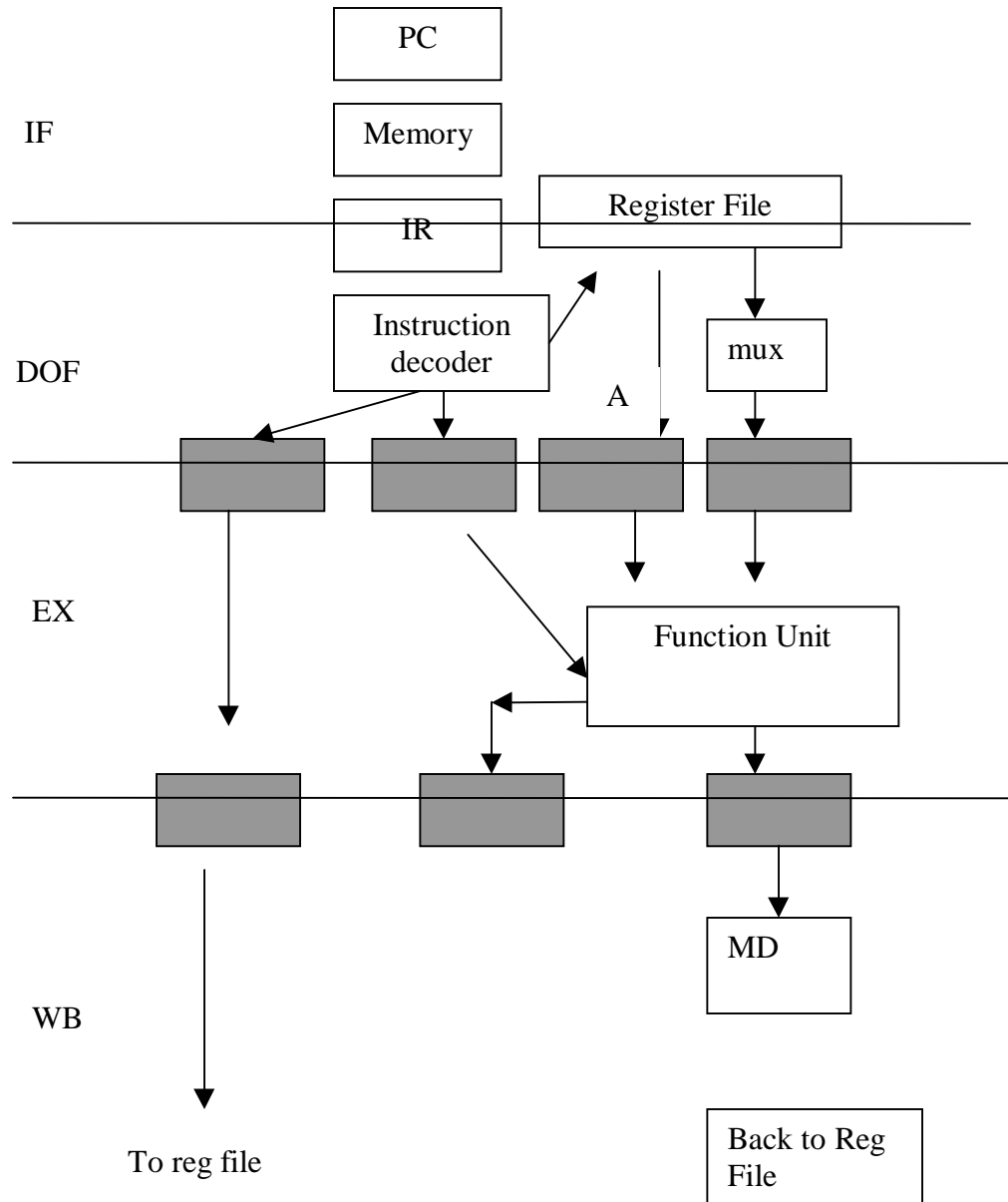- Set only by IF

PI: inc PC

- Set only by IF

PL: load PC

- Set by branch instructions

See P444 for details of IF, EXPO micro-op

Pipeline Control

- Need registers to hold control signal as the instruction moves through the pipe
- We will add another stage: instruction Fetch
- Decode can be done in the same cycle as operands fetch

	PC
IF	**Memory**
	IR **Register File**

Instruction decoder

DOF   **A**   **mux**

EX   **Function Unit**

WB

To reg file

MD

Back to Reg File

Pipeline Examples

In our example pipeline we could do these instructions:
1. R1←10
2. R2←R3 +4
3. PC← PC+6

	1	2	3	4	5	6
1	IF	DOF	EX	WB		
2		IF	DOF	EX	WB	
3			IF	DOF	EX	WB

− After the pipeline fill (3 cycles_ one instruction is completed per cycle
   o But the cycle can be ~1/4 long

What about these instructions?
1. R1←10
2. R2←5
3. PC← R1+ R2

	1	2	3	4	5	6
1	IF	DOF	EX	WB		
2		IF	DOF	EX	WB	
3			IF	DOF		

Fetch R1, R2, needs to
finish first

− This is a hazard
   o Happens any time a process is pipelined
   o The instruction with the hazard (3) must wait for the other to finish