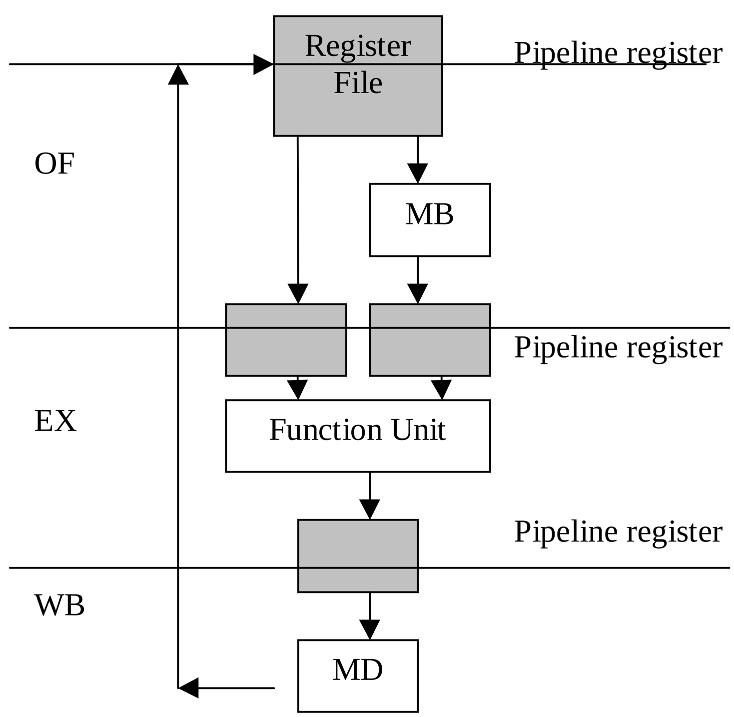
Other Choices

- Hardwired multiple cycle control
- More control memory
    - o We had 128 opcode & 256 possible microinstructions
    - o More control memory would allow more complicated micro-programs
    - o We would need to use a wider CAR
    - o More private registers
        - ▪ We had only one (R8)
        - ▪ Eg. The multiplier needs two
        - ▪ Would allow micro program that do more
    - o The single-cycle CPU could have used microprogramming
        - ▪ Instead of the decoder
    - o More advanced control select eg. Branch if less than needs N XOR V

Pipelining

- In order to do and operation with the data path we created, we have a long propagation delay
    - o The calculation must propagate through the register file, multiplexers & function unit
    - o So we need a low clock frequency
    - o We could split a micro-op across several cycles & increase the clock speed
        - ▪ Each part of the data path will do its part in one cycle
        - ▪ The parts will be separated by registers & can work independently
        - ▪ So several operations can be in progress at a time
        - ▪ Eg. Our single cycle data path with 3 stages:



- The data path has been split into 3 stages:
    - OF: operand fetch
    - EX: execute
    - WB: write back
- Each stage can be working on a different operation.
    - So we can still finish one micro op per cycle
    - If the stages are even, we can triple the clock speed (almost)
        - So the processor can do ~ 3 times as many instructions in a given time
- A little propagation delay is introduced by the pipelining registers.
    - So the best possible improvement will be <3 times
- We complete one result per cycle, but each one takes 3 cycles to finish,
    - So you can't use the result of a calculation for 3 cycles

Pipelined control

- We must make the control unit follow the timing in the data path
    - We must time the control signals so they are sent correctly
- We can add some registers to hold the control signals until needed
- Another stage will also be added" IF, instruction fetch