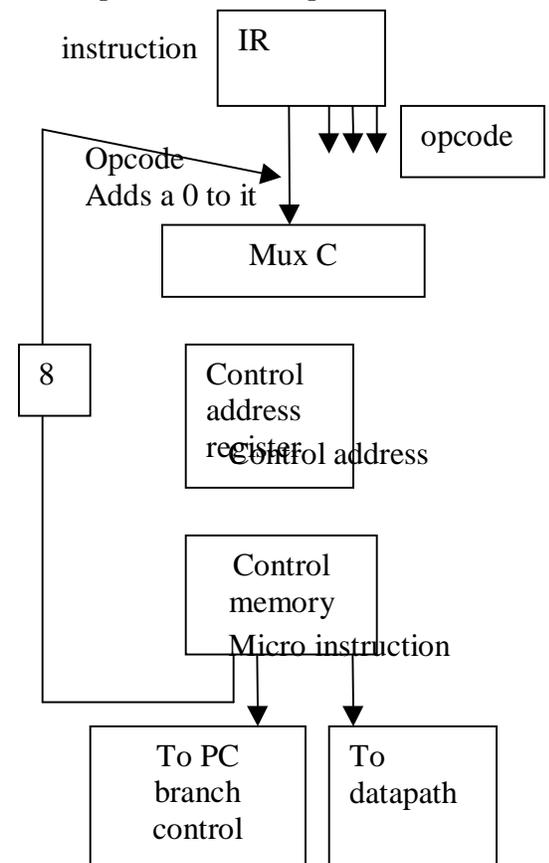


Micro-Programming

Instruction Execution:

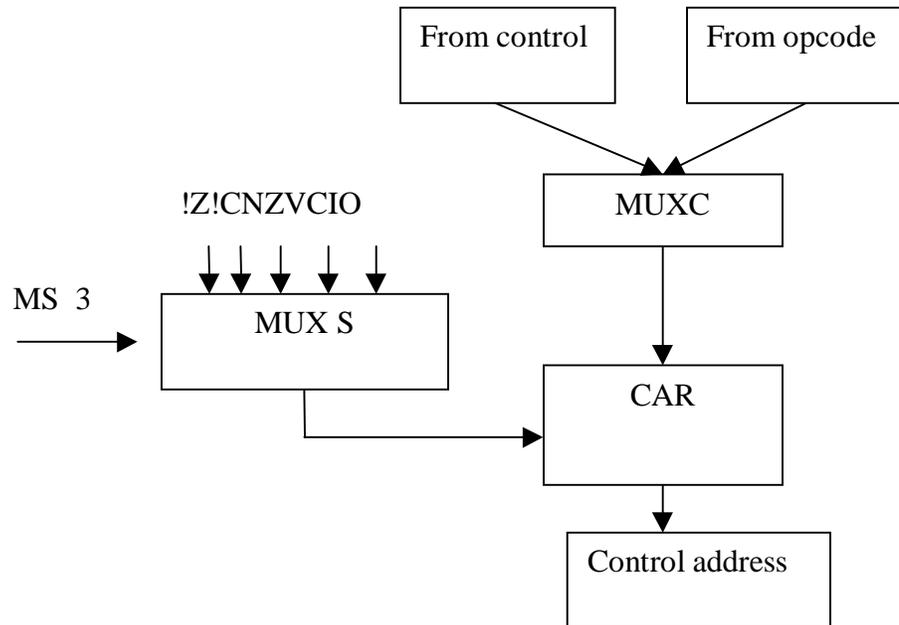
- Address from PC
- Lookup instruction in memory
- Execute
 - o If we are doing micro-programming run the micro-program for that opcode.
 - o Microinstruction execution:
- Control address from?
 - o Look up microinstruction in control memory
- Execute
 - o Send out control signals
- Where does the control address come from??
 - o In the first cycle of an instruction it's the opcode with a 0 (in the example)
 - o In the next cycle(s), it will be specified as part of the previous microop

- To start executing the instruction in the IR, set $MC \leftarrow 1$
- To execute the next microinstruction set $MC \leftarrow 0$
 - Control address of next microop specified in the previous microop



Micro-programs & status Bits

- We need to be able to check the status bits as part of a micro-program
 - o To implement conditional branch instructions
 - o Also to let the status of previous calculations
- We will let the status bits control the CAR (control address register)
 - o The CAR will either load or increment in each cycle, depending on the value of its control signal
 - o That will allow micro-programs to branch selectively
 - o A mux will let it select the branch condition



- If MUXS outputs is 0, then CAR will increment
- If MUXS outputs is 1, it will load
- The MS Signal will be another output of the control ROM
 - o Ie part of the micro instruction
- Example instruction: shift & increment
 - o First cycle: shift left
 - o MB=?
 - o FS=11000
 - o MD= 0
 - o RW=1
 - o NA= address of second microinstruction
 - o MC=0
 - o MS=001 (CAR should load)
 - o IL=0 (don't fetch)
 - o PI=1 (increment PC)
 - o PL=0 (don't load PC)

DATAPATH CONTROL STUFF

DATAPATH CONTROL STUFF

- Second cycle: increment
 - o FS= 000001(?)
 - o
 - o
 - o NA=control address of fetch microop
 - o MC=0, MS=001, IL=0
 - o PI=0, PL=0
- Third cycle: fetch
 - o IL =1;
 - o MC=1;
 - o MS=001;