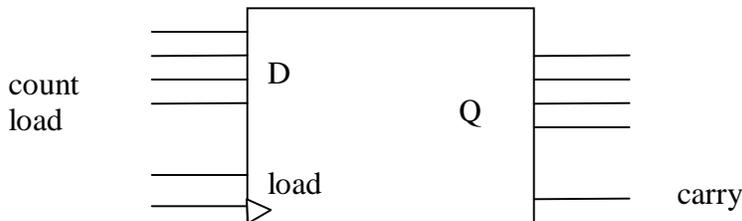


A counter in VHDL

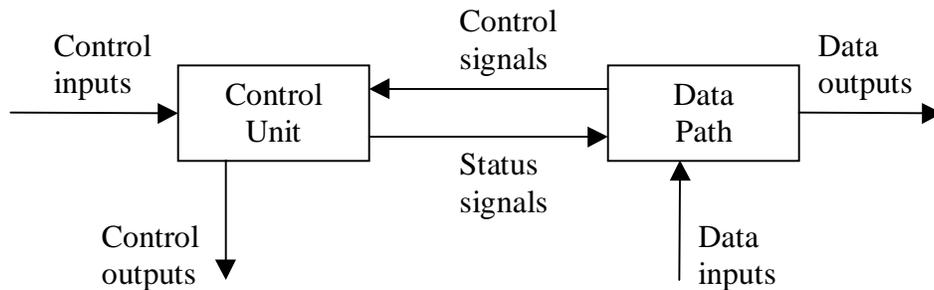
- Counter: a register that can also increment
- The circuit (drawing)



- The `std_logic_unsigned` library allows arithmetic operations to be done on `std_logic_vector` values
 - o Values are treated as unsigned integers
 - o Ie. 1111_2 is 15_{10} not -1_{10}
 - o Operations defined: + - * shifts comparisons
- In VHDL, you can't read the value of an output port
 - o `Q_int` will be an internal copy of `Q` that we can read
 - o We need to read the value to increment it
- "here" was created for testing
 - o it should be removed from the final model
- `count_process` handles parallel load & increment
 - o doesn't update `Q`, just `Q_int`
 - o line 34 does the increment.
 - o Could also have been done other ways:
 - o `Q_int <= Q_int +`
`conv_std_logic_vector (1,4)`
[convert 1 to a 4 bit value]
- `Q_update` process copies `Q_int` to `Q` when necessary.
- If the increment was above the "if", it would still work correctly
- Delta delay
 - o Signal assignments with no "after..." part have a "delta delay"
 - o Any lines of code that follows run before the signal changes
 - o Eg
 - `a <= '0'`
 - wait for 10 ns;
 - `a <= '1'`;
 - `b <= a`;
 - o At the end, `b` is '0'
 - o Signal assignments happen at the end of each "simulation cycle"

Register Transfers

- The control & datapath make up the CPU
 - o The data path performs operations on the data.
 - o The control activates the operations in the datapath



- Operations that the datapath can do in one cycle are “micro operations”
 - o Load, add, shift
- The control unit directs the datapath to do the right microop
- We will have a “register transfer language” to describe microops
 - o Eg
 - o $R1 \leftarrow R2, R2 \leftarrow R1$
(swapping content at the same time)
- Common operations
 - o + - * /
 - o AND, OR, XOR, NOT
 - o Shift right, shift left
 - o || concatenation
 - o eg.
 - o $R1 \leftarrow \text{“0000”} || R0$
(extend R0 by 4 bits, put into R1)
 - o $R2 \leftarrow R0 + R1 + 1$
(two’s compliment $R0 - R1$ into R2)
 - o $Cout || R1 \leftarrow R0 || Cin$
(shift R0 left into R1, with carry)