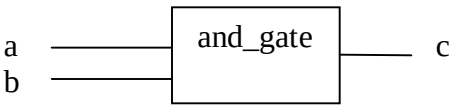
Lecture #3
May 9

```
library ieee;
use ieee.std_logic_1164.all;
entity and_gate is
        port(
                a, b    : in std_logic;
                c       : out std_logic
                );
end and_gate;
```

- Std_logic type
  - Used to represent a one bit signal
  - … or current on a signle connection
  - values:
    - ‘0’ 0—false
    - ‘1’ 1—true
    - ‘X’ error | unknown | impossible
    - ‘U’ uninitialised
  - we have now defined this block:



- entity descriptions
  - we still need to indicate that the entity does
  - an “architecture” describes how ‘its’ constructed / how it hbehaves
- there are two ways to give an architecture:
  - structural: how it is built from smaller pieces
  - behavioural: how does it behave? (don’t worry about construction)
- a behavioural architecture for the and_gate

```
architectureal behave of and_gate is
begin
        and_process: process (a,b)
        begin
                c<= a and b after 2 ns;
        end process;
end behave;
```

- give a description named “behave” of the and_gate
- it contains one “process” named “and_process”
  - a process is a (partial) description of the behaviour
  - this process depends on signals a,b

        - rerun the process whenever a or b changes
    - separate process are run concurrently (at the same time)
- the process contains one “sequential statement”
    - the statements are executed one-at-a-time
- this statement modifies the signal c
    - the <= operator is used to assign values to signals
    - “and” is defined by the IEEE library
    - it takes 2ns (nanoseconds) for the change to be visible
        - represents the propagation delay of the circuit
        - the “after..” part is optional