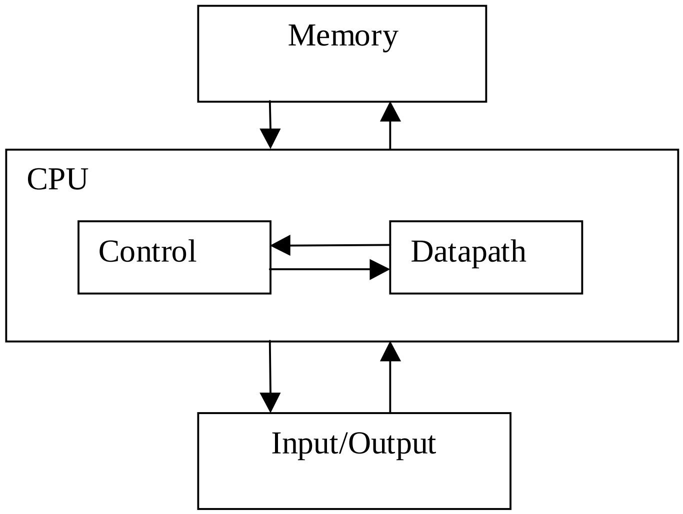
Lecture #2
May 7

Computer Strucutre

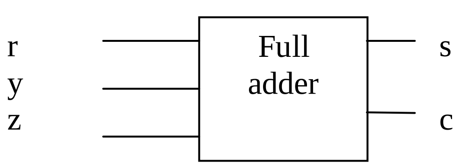
- A generic computer has 4 main units: (fig 1.2)

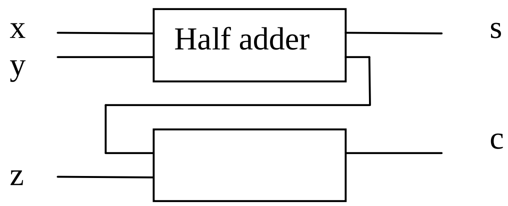


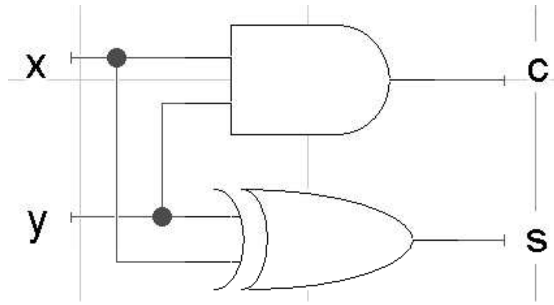
- A modern processor contains more than just the CPU. Generally:
  - The cpu: fetches & executes operations
  - The FPU (floating-point unit): like CPU, but designed for floating point operations
  - Internal cache: fast memory, used to cache main memory
  - MMU (memory management unit): manages virtual memory
- Not al processor has all of these
  - Embedded system, game machines, tec

Circuit Design

- Combinatorial circuits: outputs depend only on current iinputs
- Sequential circuits: have some kind of memory
- Hierachial design
  - Design is divided int “blocks” that can be designed separately
  - The works can than be combined
  - If we choose the right blocks, they can be re-used
    - … or they can come pre0defined in libraries
  - a full adder

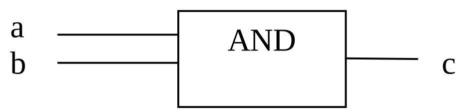






VHDL

- the “VHSIC hardware Description Language”
  - VHSIC: very high speed intergrated circuits –a US gov’t research project
- A standard language w/ many implementations
  - We’ll use synopsys
- A language for describing hardware
  - Encourages hierarchial design
  - A simple block



(an AND gate)

  - Each block is a VHDL entity
- A VHDL entity should start with these lines
  Library ieee;
  Use ieee.std_logic_1146.all;
  (grab these libraries we need)
- Then define the inputs & outputs of the block”:

```
Entity and.gate is
        port (
                a, b    : in std.loic;
                c       : out std.logic);
end and.gate;
```

- Each statement ends with a “;”
- “and gate” is the name of the entity
- “port” gives the list of ports-connections to the outside
- “a,b” are input ports, “c” is an output
- “std.logic” is a signal type that comes with the IEEE library
- signals
  - represents a signal sent along a connection
  - we’ll use std_logic for most signals
  - a std)logic signal can have these values
    - ‘0’ 0—false
    - ‘1’ 1—true
    - ‘X’ error | unknown
    - ‘U’ uninitialised
    - and 4 others