HC-11 ASSEMBLY LANGUAGE SUMMARY

MODES: XX(Y) denotes the opcode XX in hex and Y bytes/instruction

INST	FUNCTION	INH	IMM	DIR	EXT	INDX	REL
ADDA	A <- A + (M)		8B(2)	9B(2)	BB(3)	AB(2)	
ADDB	B <- B + (M)		CB(2)	DB(2)	FB(3)	EB(2)	
BRA	PC <- "addr"						20(2)
BLS	If C∨Z Then PC <- "addr"						23(2)
BSR	PC <- "addr", M[SP-1,SP] <- "return addr"						8D(2)
CLRA	A <- 0	4F(1)					
CLRB	B <- 0	5F(1)					
CMPA	If A<(M) Then C<-1, if A=(M) Then Z<-1		81(2)	91(2)			
CMPB	If B<(M) Then C<-1, if B=(M) Then Z<-1		C1(2)	D1(2)			
CPX	If X=(M,M+1) Then Z<-1		8C(3)	9C(2)	BC(3)	AC(2)	
DES	SP <- SP-1	34(1)					
DEX	X <- X-1	09(1)					
INS	SP <- SP + 1	31(1)					
LDAA	A <- (M)		86(2)	96(2)	B6(3)	A6(2)	
LDAB	B <- (M)		C6(2)	D6(2)	F6(3)	E6(2)	
LDX	X <- (M,M+1)		CE(3)	DE(2)	FE(3)		
LDY	Y <- (M, M+1)						
MUL	D <- A*B	3D(1)					
PSHA	M[SP]<- A,SP <- SP-1	36(1)					
PSHB	M[SP]<- B,SP <- SP-1	37(1)					
PSHX	M[SP] <-X(LO), M[SP-1] <- X(HI), SP<- SP+2	3C(1)					
PSHY	M[SP] <-Y(LO), M[SP-1] <- Y(HI), SP<- SP+2						
PULA	A <- M[SP+1], SP<- SP+1	32(1)					
PULB	B <- M[SP+1], SP<- SP+1	33(1)					
PULX	X(HI) <- M[SP+1], X(LO) <- M[SP+2], SP<- SP+2	38(1)					
PULY	Y(HI) <- M[SP+1], Y(LO) <- M[SP+2], SP<- SP+2						
RTS	PC <- M[SP+1,SP+2], SP<- SP+2	39(1)					
STAA	M <- A			97(2)	B7(3)	A7(2)	
STAB	M <- B			D7(2)	F7(3)	E7(2)	
STOP	"stop"	CF(1)					
STX	M <- X(HI), M+1 <- X(LO)			DF(2)	FF(3)	EF(2)	
SUBA	A <- A - (M)		80(2)	90(2)	B0(3)	A0(2)	
SUBB	B <- B - (M)		C0(2)	D0(2)	F0(3)	E0(2)	
TSX	X <- SP+1		30(1)				
TSY	Y <- SP+1						

NOTES:

1. For all branch instructions "addr" is obtained by adding the displacement stored in the instruction to the address of the current instruction and then adding 2.
2. Not all addressing modes have been identified for the instructions given; only those modes that may be needed for this test.
3. M defines an address in memory. Its value depends on the addressing mode used. (M) denotes the contents of that memory location, while M[] (eg., M[SP]) denotes the address in memory specified by the register in square brackets (i.e., SP). M[U,V] specifies two locations of memory, namely those given by the value of U and V.
4. The following modes are identified. No entry in the row and column for a given instruction signifies that the mode is not available for that instruction.
    a. INH: Inherent
    b. IMM: Immediate
    c. DIR: Direct (as defined for HC-11)
    d. EXT: Extended
    e. INDX: Indexed using register X
    f. REL: Relative
5. The opcodes for instructions that access the Y register are 2 bytes long and have not been included explicitly. You may assume the same modes exist as for the corresponding instructions using the X register.