Lecture 21 June 25

Hazards

- If an instruction tries to access a register that will be modified by an instruction in the pipeline
 - o This is a "data hazard"
 - o Ex
 - 1. R2←10
 - 2. $R2 \leftarrow R1 + R2$
 - note: in the example architecture, the WB and DOF can be done in the same cycle
 - if there was an instruction between the ones above, no hazard
- a hazard can also occur when the programmer requests a conditional branch
 - o ex
- I. BRZset
- ADD
- Instruction 2 would be inserted into the pipeline before 1 is finished
- If the branch is taken, it shouldn't be executed
- o A "control hazard"
- Possible solution 1: Do nothing
 - Make the programmer/compiler figure it out
 - o No change in the circuits, just warn the programmer
 - o Need to add a NOP (no operation) instruction
 - o EX



- this requires the programmer/compiler to know a lot about the underlying architecture
- makes it hard to program
- o no chance of backward compatibility with older code
- Possible solution 2: stall
 - Have the processor delay an instruction when necessary
 - When the processor notice a hazard it launches a "bubble"
 - I.e. keeps the instruction from moving down the pipe

o E.g.

Launches bubble

R1←10:	IF	DOF	EX	WB				
R2 ← R1+R2:		IF	DOF	0	0			
				DOF	EX	WB	\mathbf{N}	
R1←R2+1:				IF	DOF	0	0	
						DOF	EX	WB

Notice hazard

- Designing a control unit to do this is tricky
 - Must check DR of instruction in the pipe
 - If they correspond to an operand in the pipe (current instruction), stall
 - To stall: in the next cycle, send the same instruction through the pipe
 - Don't increment PC or update IR
 - We must make sure the bubble has RW=MW=0
 - So it doesn't have any effect
 - For a control hazard, we don't want to always do the next instruction
 - More later
- Possible Solution 3: data forwarding (for data hazards only)
 - o If the data is already in the pipeline somewhere use if from there

0	E.g.
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R1 ← 10:	IF	DOF	EX	WB	
$R2 \leftarrow R1 + R2$		IF	DOF	EX	WB

Get the RI value from the function unit, not reg. file